Memec Mini-Module Specification (version 0.5)

FEATURES

- **Complete FPGA System-on-a-module**
- **Supports FPGA-based embedded processors**
  - **Xilinx PowerPC (Virtex-4 only)**
  - **Xilinx MicroBlaze (Virtex and Spartan families)**
- **Ethernet interface with RJ45 connector**
- **RAM**
- **Flash memory**
- **76 user defined I/O signal pins**
- **FPGA non-volatile configuration code storage**
- **Small form factor (30 mm x 65.5 mm / 1.2" x 2.6")**
- **Single ended and differential signaling support**
- **On-board clock source**

APPLICATIONS

- **MicroBlaze and/or PowerPC based systems**
- **Embedded controller**
- **Industrial controller**
- **Internet appliance**
- **Communications processing**
- **Prototyping and low-volume production systems**

DESCRIPTION

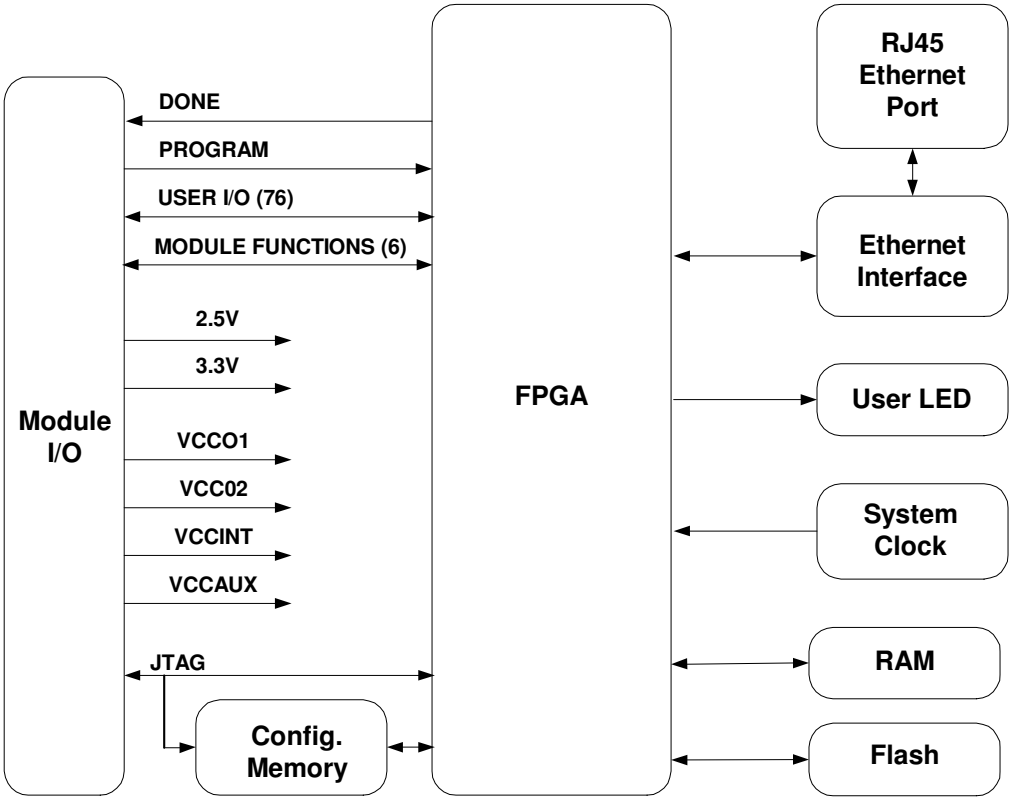
The Memec Mini-Module is a complete FPGA system-on-a-module, ideal for embedded processor applications and general programmable systems applications. The Mini-Module is a small plug-in board, containing a Xilinx FPGA, configuration memory, RAM, parallel Flash memory, an Ethernet port, a clock source and a user LED. The module provides 76 user definable IO pins through the 2x32 pin headers along each side of the circuit board. The module connects via a socket or thru-hole mounting to a baseboard, which provides the various module power requirements, JTAG interfaces, some status and control, and any user application circuitry. The module integrates all fine pitch components required for most systems, thus simplifying the design of the baseboard and lowering the over-all system cost.

This document provides the general Mini-Module specifications that are common to all Mini-Modules. The detail of each module's unique functionality is provided in the respective Mini-Module User Guide.

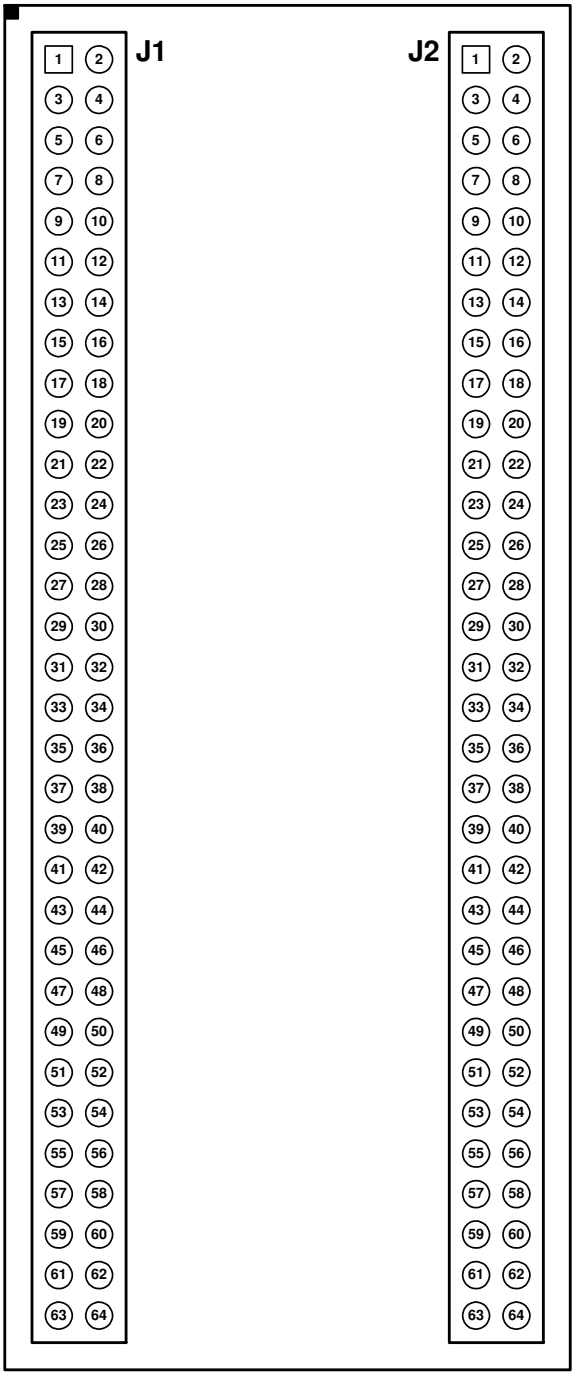
ORDERING INFORMATION

PRODUCT	ORDERING NUMBER
Spartan-3 Mini-Module ✓ 3S400-FT256 FPGA ✓ 256k x 32 IDT SRAM ✓ 1M x 16 Atmel Flash ✓ 10/100 SMSC MAC/PHY ✓ CPLD/Serial Data Flash FPGA code storage	DS-KIT-3S400MM1
Virtex-4 FX12 Mini-Module ✓ 4VFX12-SF363 FPGA ✓ 32M x 16 DDR SDRAM ✓ 2M x 16 Atmel Flash ✓ 10/100/1000 Broadcom PHY ✓ Platform Flash PROM FPGA code storage	DS-KIT-FX12MM1

BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

PIN ASSIGNMENTS (J1)

Pin #	Type	Direction	Signal Name	Description
J1-1	KEY	-	KEY	Connector keying (no pin)
J1-2	POWER	-	VCCINT	FPGA core voltage supply
J1-3	POWER	-	VCCINT	FPGA core voltage supply
J1-4	POWER	-	VCCINT	FPGA core voltage supply
J1-5	POWER	-	GND	Ground
J1-6	POWER	-	GND	Ground
J1-7	MDF	(1)	MDF1	Module Defined Function 1
J1-8	MDF	(1)	MDF2	Module Defined Function 2
J1-9	MDF	(1)	MDF3	Module Defined Function 3
J1-10	MDF	(1)	MDF4	Module Defined Function 4
J1-11	POWER	-	GND	Ground
J1-12	POWER	-	GND	Ground
J1-13	CONF	OUT	DONE	FPGA DONE signal
J1-14	MDF	(1)	MDF5	Module Defined Function 5
J1-15	POWER	-	GND	Ground
J1-16	POWER	-	GND	Ground
J1-17	POWER	-	2.5V	2.5V
J1-18	POWER	-	2.5V	2.5V
J1-19	SE	IN/OUT	IO_1_00	User definable single-ended signal
J1-20	SE	IN/OUT	IO_1_01	User definable single-ended signal
J1-21	SE	IN/OUT	IO_1_02	User definable single-ended signal
J1-22	SE	IN/OUT	IO_1_03	User definable single-ended signal
J1-23	POWER	-	2.5V	2.5V
J1-24	POWER	-	2.5V	2.5V
J1-25	POWER	-	GND	Ground
J1-26	POWER	-	GND	Ground
J1-27	SE/DIFF	IN/OUT	IO_1_04_1P	User definable signal
J1-28	SE/DIFF	IN/OUT	IO_1_05_1N	User definable signal
J1-29	SE/DIFF	IN/OUT	IO_1_06_2P	User definable signal
J1-30	SE/DIFF	IN/OUT	IO_1_07_2N	User definable signal
J1-31	SE/DIFF	IN/OUT	IO_1_08_3P	User definable signal
J1-32	SE/DIFF	IN/OUT	IO_1_09_3N	User definable signal
J1-33	SE/DIFF	IN/OUT	IO_1_10_4P	User definable signal
J1-34	SE/DIFF	IN/OUT	IO_1_11_4N	User definable signal
J1-35	SE/DIFF	IN/OUT	IO_1_12_5P	User definable signal
J1-36	SE/DIFF	IN/OUT	IO_1_13_5N	User definable signal
J1-37	SE/DIFF	IN/OUT	IO_1_14_6P	User definable signal
J1-38	SE/DIFF	IN/OUT	IO_1_15_6N	User definable signal
J1-39	SE/DIFF	IN/OUT	IO_1_16_7P	User definable signal
J1-40	SE/DIFF	IN/OUT	IO_1_17_7N	User definable signal
J1-41	SE/DIFF	IN/OUT	IO_1_18_8P	User definable signal
J1-42	SE/DIFF	IN/OUT	IO_1_19_8N	User definable signal
J1-43	POWER	-	GND	Ground
J1-44	POWER	-	GND	Ground
J1-45	SE/DIFF/DCLK	IN	I_1_20_CLKP	User clock input
J1-46	SE/DIFF/DCLK	IN	I_1_21_CLKN	User clock input
J1-47	POWER	-	VCCO1	J1 signal level voltage (2.5V or 3.3V)
J1-48	POWER	-	VCCO1	J1 signal level voltage (2.5V or 3.3V)
J1-49	SE/DIFF	IN/OUT	IO_1_22_9P	User definable signal
J1-50	SE/DIFF	IN/OUT	IO_1_23_9N	User definable signal
J1-51	SE/DIFF	IN/OUT	IO_1_24_10P	User definable signal
J1-52	SE/DIFF	IN/OUT	IO_1_25_10N	User definable signal
J1-53	SE/DIFF	IN/OUT	IO_1_26_11P	User definable signal
J1-54	SE/DIFF	IN/OUT	IO_1_27_11N	User definable signal
J1-55	SE/DIFF	IN/OUT	IO_1_28_12P	User definable signal
J1-56	SE/DIFF	IN/OUT	IO_1_29_12N	User definable signal
J1-57	SE/DIFF	IN/OUT	IO_1_30_13P	User definable signal
J1-58	SE/DIFF	IN/OUT	IO_1_31_13N	User definable signal
J1-59	SE/DIFF	IN/OUT	IO_1_32_14P	User definable signal
J1-60	SE/DIFF	IN/OUT	IO_1_33_14N	User definable signal
J1-61	SE/DIFF	IN/OUT	IO_1_34_15P	User definable signal
J1-62	SE/DIFF	IN/OUT	IO_1_35_15N	User definable signal
J1-63	SE/DIFF	IN/OUT	IO_1_36_16P	User definable signal
J1-64	SE/DIFF	IN/OUT	IO_1_37_16N	User definable signal

(1) - The direction of this pin is dependent on the module function

PIN ASSIGNMENTS (J2)

Pin #	Type	Direction	Signal Name	Description
J2-1	KEY	-	KEY	Connector keying (no pin)
J2-2	POWER	-	VCCAUX	FPGA auxiliary voltage supply
J2-3	POWER	-	VCCAUX	FPGA auxiliary voltage supply
J2-4	POWER	-	VCCAUX	FPGA auxiliary voltage supply
J2-5	POWER	-	GND	Ground
J2-6	POWER	-	GND	Ground
J2-7	JTAG	IN	TMS	Primary JTAG TEST MODE SELECT
J2-8	JTAG	OUT	TCK	Primary JTAG TEST CLOCK
J2-9	JTAG	IN	TDI	Primary JTAG TEST DATA IN
J2-10	JTAG	IN	TDO	Primary JTAG TEST DATA OUT
J2-11	POWER	-	GND	Ground
J2-12	POWER	-	GND	Ground
J2-13	MDF	(1)	MDF6	Module Defined Function 6
J2-14	CONF	IN	PROGRAM	FPGA program signal
J2-15	POWER	-	GND	Ground
J2-16	POWER	-	GND	Ground
J2-17	POWER	-	3.3V	3.3V
J2-18	POWER	-	3.3V	3.3V
J2-19	SE	IN/OUT	IO_2_00	User definable single-ended signal
J2-20	SE	IN/OUT	IO_2_01	User definable single-ended signal
J2-21	POWER	-	3.3V	3.3V
J2-22	POWER	-	3.3V	3.3V
J2-23	POWER	-	GND	Ground
J2-24	POWER	-	GND	Ground
J2-25	SE	IN/OUT	IO_2_02	User definable single-ended signal
J2-26	SE	IN/OUT	IO_2_03	User definable single-ended signal
J2-27	SE	IN/OUT	IO_2_04	User definable single-ended signal
J2-28	SE	IN/OUT	IO_2_05	User definable single-ended signal
J2-29	SE	IN/OUT	IO_2_06	User definable single-ended signal
J2-30	SE	IN/OUT	IO_2_07	User definable single-ended signal
J2-31	SE	IN/OUT	IO_2_08	User definable single-ended signal
J2-32	SE	IN/OUT	IO_2_09	User definable single-ended signal
J2-33	SE	IN/OUT	IO_2_10	User definable single-ended signal
J2-34	SE	IN/OUT	IO_2_11	User definable single-ended signal
J2-35	SE	IN/OUT	IO_2_12	User definable single-ended signal
J2-36	SE	IN/OUT	IO_2_13	User definable single-ended signal
J2-37	SE	IN/OUT	IO_2_14	User definable single-ended signal
J2-38	SE	IN/OUT	IO_2_15	User definable single-ended signal
J2-39	SE	IN/OUT	IO_2_16	User definable single-ended signal
J2-40	SE	IN/OUT	IO_2_17	User definable single-ended signal
J2-41	POWER	-	GND	Ground
J2-42	POWER	-	GND	Ground
J2-43	SE/CLK	IN/OUT	IO_2_18_CLK0	User definable signal
J2-44	SE/CLK	IN/OUT	IO_2_19_CLK1	User definable signal
J2-45	SE/DIFF/DCLK	IN	I_2_20_CLKP	User definable signal, clock input
J2-46	SE/DIFF/DCLK	IN	I_2_21_CLKN	User definable signal, clock input
J2-47	POWER	-	VCCO2	J2 signal level voltage (2.5V or 3.3V)
J2-48	POWER	-	VCCO2	J2 signal level voltage (2.5V or 3.3V)
J2-49	SE	IN/OUT	IO_2_22	User definable single-ended signal
J2-50	SE	IN/OUT	IO_2_23	User definable single-ended signal
J2-51	SE	IN/OUT	IO_2_24	User definable single-ended signal
J2-52	SE	IN/OUT	IO_2_25	User definable single-ended signal
J2-53	SE	IN/OUT	IO_2_26	User definable single-ended signal
J2-54	SE	IN/OUT	IO_2_27	User definable single-ended signal
J2-55	SE	IN/OUT	IO_2_28	User definable single-ended signal
J2-56	SE	IN/OUT	IO_2_29	User definable single-ended signal
J2-57	SE	IN/OUT	IO_2_30	User definable single-ended signal
J2-58	SE	IN/OUT	IO_2_31	User definable single-ended signal
J2-59	SE	IN/OUT	IO_2_32	User definable single-ended signal
J2-60	SE	IN/OUT	IO_2_33	User definable single-ended signal
J2-61	SE	IN/OUT	IO_2_34	User definable single-ended signal
J2-62	SE	IN/OUT	IO_2_35	User definable single-ended signal
J2-63	SE	IN/OUT	IO_2_36	User definable single-ended signal
J2-64	SE	IN/OUT	IO_2_37	User definable single-ended signal

(1) - The direction of this pin is dependent on the module function

SIGNAL NAME DESCRIPTION

The following defines the user signal naming convention of the Mini-Modules:

```
PINTYPE _ BANK _ SE SIGNAL# [ _ CLOCK OR LVDS SIGNAL ]
|         |      |                |
|         |      |                CLKn FOR SINGLE-ENDED CLOCK CAPABLE
|         |      |                CLKP FOR DIFFERENTIAL CLOCK CAPABLE (POSITIVE LINE)
|         |      |                CLKN FOR SINGLE-ENDED CLOCK CAPABLE (NEGATIVE LINE)
|         |      |                nnP FOR LVDS CAPABLE SIGNAL (POSITIVE LINE)
|         |      |                nnN FOR LVDS CAPABLE SIGNAL (NEGATIVE LINE)
|         |      |
|         |      nn = SINGLE-ENDED SIGNAL NUMBER
|         |
|         1 = SIGNAL IS ON J1
|         2 = SIGNAL IS ON J2
|
I = INPUT
O = OUTPUT
IO = BIDIRECTIONAL
```

EXAMPLE #1

IO_2_18_CLK0 is a user I/O signal located on J2. It can be defined as a single-ended user I/O (i.e. number 18), but can also be used as a clock input to the FPGA since it is connected to a global clock pin on the FPGA. The 2.5V or 3.3V voltage level for this pin is defined by the value of the VCCO pins on J2.

```
IO _ 2 _ 18 _ CLK0
|    |   |     |
|    |   |     CLK0 = OPTIONAL CLOCK INPUT #0
|    |   |
|    |   18 = SINGLE-ENDED SIGNAL #18
|    |
|    2 = SIGNAL IS ON J2 (SIGNAL VOLTAGE LEVEL IS VCCO2, WHERE SUPPORTED)
|
I0 = INPUT/OUTPUT
```

EXAMPLE #2

IO_1_04_1P is a user I/O signal located on J1. It can be defined as a single-ended user I/O (i.e. number 4), or as an LVDS signal (i.e. the P-side of LVDS pair #1).

```
IO _ 1 _ 04 _ 1P
|    |   |    |
|    |   |    1P = OPTIONAL POSITIVE LINE OF DIFFERENTIAL PAIR #1
|    |   |
|    |   04 = SINGLE-ENDED SIGNAL #04
|    |
|    1 = SIGNAL IS ON J1 (SIGNAL VOLTAGE LEVEL IS VCCO1, WHERE SUPPORTED)
|
IO = INPUT/OUTPUT
```

DETAILED SIGNAL DESCRIPTIONS

POWER
VCCINT -
VCCAUX -
VCCO1/2 -
2.5V -
3.3V -
GND -

PRIMARY JTAG
TMS -
TCK -
TDI -
TDO -

MODULE DEFINED FUNCTION
MDF1
MDF2
MDF3
MDF4
MDF5
MDF6

CONFIGURATION
DONE -
PROGRAM -

USER DEFINABLE SIGNALS
SE -
DIFF -
CLK -

ABSOLUTE MAXIMUM RATINGS

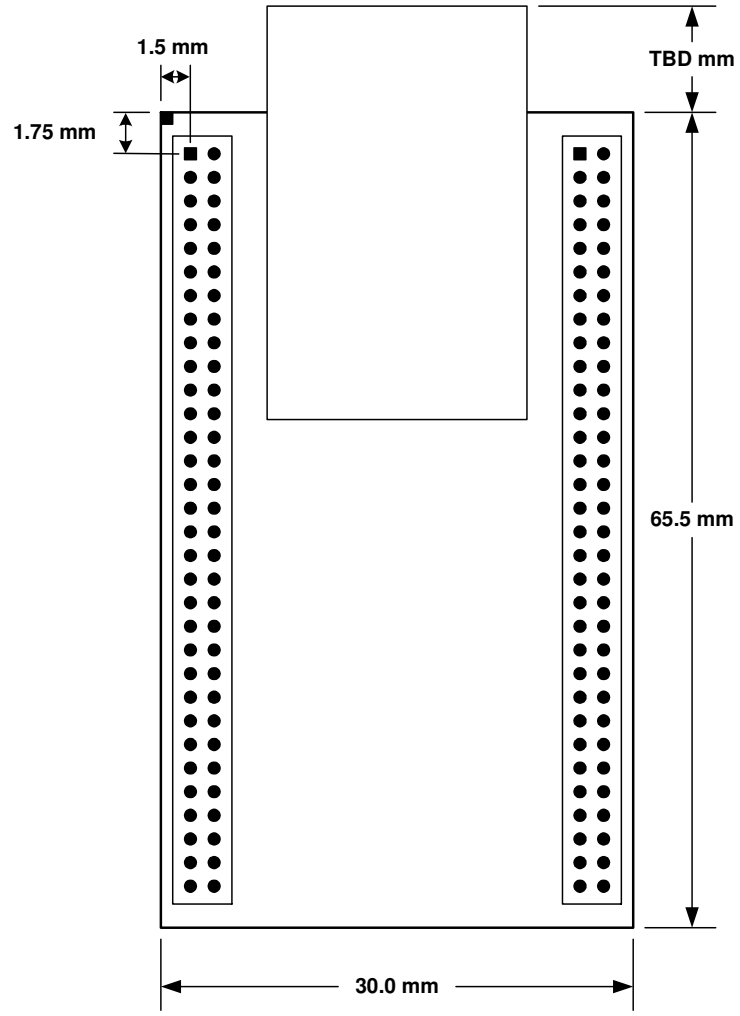
Parameter	RANGE	UNITS
		V
		mA

RECOMMENDED OPERATING CONDITIONS

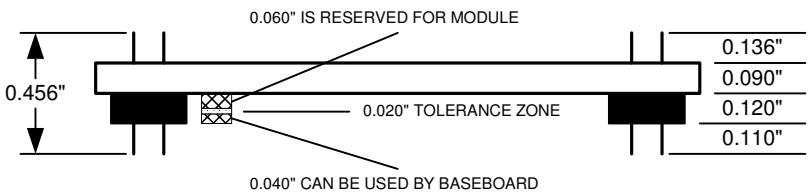
Parameter		MINIMUM	TYPICAL	MAXIMUM	UNITS
VINT	Spartan-3				V
	Virtex-4				V
VAUX					V
2.5V					V
3.3V					
VCCO1/2	2.5V				V
	3.3V				V
VINT	Spartan-3				mA
	Virtex-4				mA
VAUX					mA
2.5V					mA
3.3V					mA
VCCO1/2	2.5V				mA
	3.3V				mA

ELECTRICAL CHARACTERISTICS

MODULE DIMENSIONS

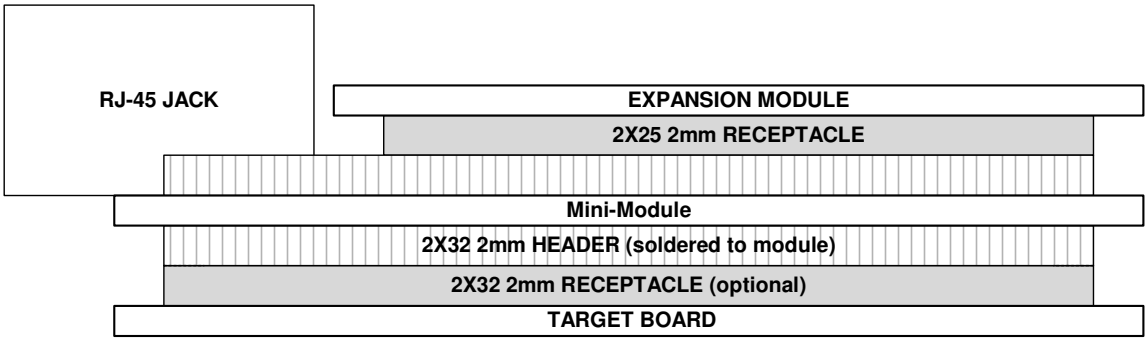


TOP VIEW



END VIEW

MODULE MOUNTING



SIDE VIEW